IN THE CLAIMS:

1. (Original) A method, comprising:

preparing a sectional sample of a portion of a conductive structure embedded in a dielectric layer of a microstructure device so as to maintain said portion embedded in said dielectric layer; and

obtaining cross-section analysis measurement data of said sectional sample by electron microscopy while subjecting said portion of said conductive structure to a specified stress condition.

2. (Original) The method of claim 1, wherein said conductive structure is comprised of a metal.

3. (Original) The method of claim 1, wherein said conductive structure is comprised of copper.

4. (Original) The method of claim 1, wherein said cross-section analysis measurement data are obtained in the form of at least one image.

5. (Original) The method of claim 1, wherein said conductive structure is formed in accordance with a predefined manufacturing sequence for said microstructure device.

6. (Original) The method of claim 5, further comprising assessing said predefined manufacturing sequence on the basis of said at least one image.

7. (Original) The method of claim 1, wherein said specified stress condition comprises generating a predefined initial current density in said metal line.

8. (Original) The method of claim 1, wherein said specified stress condition comprises heating said sectional sample.

9. (Original) The method of claim of claim 1, further comprising obtaining a plurality of images of said sectional sample and displaying said plurality of images in quick motion to visualize degradation effects of said conductive structure under said specified stress condition.

10. (Original) The method of claim 1, wherein preparing said sectional sample comprises forming a first metal line, a second metal line and an interconnect in said microstructure device, said interconnect connecting said first and second metal lines, and cutting said microstructure device and thinning a cut portion thereof to obtain said sample, wherein said sample includes said interconnect embedded in a dielectric.

11. (Original) The method of claim 10, wherein forming said first and second metal lines and said interconnect includes forming said first metal line in a first metallization layer and forming said second metal line and said interconnect commonly in a second metallization layer.

12. (Original) The method of claim 11, wherein said first and second metal lines and said interconnect comprise copper and a conductive barrier layer separating at least some of the sidewalls of said first and second metal lines and said interconnect from adjacent dielectric material.

13. (Original) The method of claim 12, wherein said conductive structure comprises a dielectric barrier layer forming an interface with copper.

14. (Original) The method of claim 1, wherein a thickness of dielectric material forming a surface over said first and second metal lines and said interconnect and being exposed to short wavelength radiation during obtaining said cross-section analysis measurement data is approximately 100 nanometer or less.

15. (Original) The method of claim 14, wherein an energy of said short wavelength radiation is selected so as to at least transmit through said thickness of said dielectric material.

16. (Original) The method of claim 5, further comprising obtaining a correlation between at least one process parameter of said predefined manufacturing sequence and said cross-section analysis measurement data.

17. (Original) The method of claim 16, further comprising:

preparing a second sectional sample of a portion of a conductive structure embedded in a dielectric of a microstructure device so as to maintain said portion embedded in said dielectric;

obtaining second cross-section analysis measurement data from said second sectional sample while subjecting said portion of said conductive structure to a specified stress condition; and

controlling said at least one process parameter on the basis of said correlation and said second cross-section analysis measurement data.

18. (Currently Amended) A method, comprising:

preparing a sectional sample of a portion of interest of a microstructure, wherein said portion of interest comprises at least one conductive structure embedded in a dielectric material;

generating a plurality of images of said sectional sample; and

displaying said plurality of images in a quick motion mode so as to assess at least one characteristic of said portion of interest.

19. (Original) The method of claim 18, wherein said plurality of images are generated by exposing said sectional sample to short wavelength radiation.

20. (Canceled)

21. (Currently Amended) The method of ~~claim 20~~ claim 18, further comprising applying a specified stress condition to said sectional sample prior to generating at least some of said plurality of images.

22. (Original) The method of claim 21, wherein applying a specified stress condition includes flowing a current through said conductive structure.

23. (Original) The method of claim 21, wherein applying a specified stress condition includes heating said sectional sample.

24. (Original) The method of claim 18, wherein said at least one characteristic includes stress-induced material transport in said conductive structure.

25. (Original) The method of claim 18, wherein said at least one characteristic includes at least one of grain size, texture and stress components in at least one specified direction.

26. (Original) The method of claim 23, wherein said conductive structure comprises a conductive barrier layer forming an interface with metal in said metal layer and with a dielectric in which said conductive structure is embedded.

27. (Original) The method of claim 26, wherein said at least one characteristic includes material transport along said interfaces.

28. (Original) The method of claim 23, wherein said metal line comprises copper.

29. (Original) The method of claim 18, further comprising obtaining a correlation between said at least one characteristic and at least one process parameter for manufacturing said microstructure.

30. (Original) The method of claim 29, further comprising controlling said at least one process parameter during the fabrication of at least one further microstructure including said portion of interest on the basis of said correlation.

31. (Original) The method of claim 18, wherein said portion of interest includes at least one metal line and wherein said sample is prepared so as to maintain said at least one metal line embedded in said dielectric.

32. (Original) The method of claim 31, wherein preparing said sectional sample includes maintaining at least one surface of said dielectric that is exposed to the short wavelength radiation with a thickness of 100 nanometer or less.

33. (Original) The method of claim 19, wherein said short wavelength radiation is comprised of an electron beam.

34. (Original) A method, comprising:

preparing a sectional sample of at least a portion of an interconnect structure positioned in a dielectric layer;

obtaining a plurality of images of at least said portion of said interconnect structure while subjecting said portion of said interconnect structure to a specific stress condition; and

displaying said plurality of images in quick motion to visualize degradation effects on said interconnect structure under said stress conditions.

35. (Original) The method of claim 34, wherein said interconnect structure is a metal line.

36. (Original) The method of claim 34, wherein said interconnect structure is comprised of copper.

37. (Original) The method of claim 34, wherein said plurality of images is obtained by at least one of scanning electron microscopy and x-ray microscopy.

38. (Original) A sectional sample of a portion of interest of a microstructure, comprising:

a first elongated metal region having a first longitudinal axis;

a second elongated metal region having a second longitudinal axis, the first and second metal regions connected to each other so as to form a substantially right angle with first and second longitudinal axis; and

a dielectric material enclosing said first and second metal regions, said dielectric material forming a layer having at least one exposed surface above said first and second metal regions, wherein a thickness of said layer is approximately 100 nanometer or less for scanning electron microscopy studies.

39. (Original) The sectional sample of claim 38, wherein said first and second metal regions comprise a conductive barrier layer in contact with said dielectric material.

40. (Original) The sectional sample of claim 38, wherein said first and second metal regions comprise copper.

41. (Original) The sectional sample of claim 38, wherein at least one of said first and second metal regions comprises a dielectric capping layer in contact with said copper.

42. (New) The method of claim 1, wherein said conductive structure has a plurality of side surfaces and a plurality of end surfaces, wherein said dielectric layer encapsulates said side surfaces of said conductive structure.

43. (New) The method of claim 1, wherein said sectional sample comprises:

a first elongated metal region having a first longitudinal axis;

a second elongated metal region having a second longitudinal axis, the first and second metal regions connected to each other so as to form a substantially right angle with first and second longitudinal axis; and

a dielectric material enclosing said first and second metal regions, said dielectric material forming a layer having at least one exposed surface above said first and second metal regions, wherein a thickness of said layer is approximately 100 nanometer or less for scanning electron microscopy studies.

44. (New) A method, comprising:

preparing a sectional sample of a portion of interest of a microstructure, wherein said portion of interest comprises at least one conductive structure embedded in a dielectric material, said microstructure comprising:

a first elongated metal region having a first longitudinal axis,

a second elongated metal region having a second longitudinal axis, the first and second metal regions connected to each other so as to form a substantially right angle with first and second longitudinal axis, and

a dielectric material enclosing said first and second metal regions, said dielectric material forming a layer having at least one exposed surface above said first and second metal regions, wherein a thickness of said layer is approximately 100 nanometer or less for scanning electron microscopy studies;

generating a plurality of images of said sectional sample; and displaying said plurality of images in a quick motion mode so as to assess at least one characteristic of said portion of interest.

45. (New) The method of claim of claim 44, further comprising obtaining a plurality of images of said sectional sample and displaying said plurality of images in quick motion to visualize degradation effects of said conductive structure under said specified stress condition.

46. (New) A method, comprising:

preparing a sectional sample of at least a portion of an interconnect structure positioned in a dielectric layer, said interconnect structure comprising:

a first elongated metal region having a first longitudinal axis,

a second elongated metal region having a second longitudinal axis, the first and second metal regions connected to each other so as to form a substantially right angle with first and second longitudinal axis, and

a dielectric material enclosing said first and second metal regions, said dielectric material forming a layer having at least one exposed surface above said first and second metal regions, wherein a thickness of said layer is approximately 100 nanometer or less for scanning electron microscopy studies;

obtaining a plurality of images of at least said portion of said interconnect structure while subjecting said portion of said interconnect structure to a specific stress condition; and displaying said plurality of images in quick motion to visualize degradation effects on said interconnect structure under said stress conditions.

47. (New) The method of claim 46, wherein said at least one characteristic includes stress-induced material transport in said conductive structure.

48. (New) The method of claim 46, wherein said at least one characteristic includes at least one of grain size, texture and stress components in at least one specified direction.